



Shri Vaishnav Vidyapeeth Vishwavidyalaya
Shri Vaishnav Institute of Technology and Science
Choice Based Credit System (CBCS) Scheme in the light of NEP-2020
M.Tech. (VLSI Design)

SEMESTER-III (2025-2027)

S. No.	COURSE CODE	COURSE NAME	TEACHING SCHEME/WEEK			CREDITS	EXAMINATION SCHEME					TOTAL MARKS
			L	T	P		THEORY			PRACTICAL		
							End Sem University Exam (60%)	Two Term Exam (20%)	Teachers Assessment* (20%)	End Sem University Exam (60%)	Teachers Assessment* (40%)	
1	-	Elective III	3	0	0	3	60	20	20	0	0	100
2	-	Elective IV	3	0	0	3	60	20	20	0	0	100
3	-	MOOCs	2	0	0	2	-	-	-	-	-	100
4	MTVD303	Dissertation Phase I	0	0	20	10	0	0	0	180	120	300
TOTAL			8	0	20	18	120	40	40	180	120	600

Legends: L - Lecture ; T - Tutorial/Teacher Guided Student Activity ; P - Practical

*Teacher Assessment shall be based on following components: Quiz/Assignment/Project/Participation in Class, given that no component shall exceed more than 10 marks.

* Students have to compulsorily opt MOOCs course of two credit from Swayam Portal

Elective III			Elective IV		
S. No.	Course Code	Course Name	S. No.	Course Code	Course Name
1	MTVD311	Mixed Signal System Design	1	MTVD312	Product Architectures Models and Firmware
2	MTEEE321	Artificial Intelligence and Machine Learning	2	MTVD322	SOC's Design Principals for Industrial Applications
3	MTVD331	Hardware/Software Codesign	3	MTVD332	Physical Design and Graphic Design

Signature
20/1/2026

Signature
Chairperson
 Board of Studies
 Shri Vaishnav Vidyapeeth
 Vishwavidyalaya, Indore

Signature
Chairperson
 Faculty of Studies
 Shri Vaishnav Vidyapeeth
 Vishwavidyalaya, Indore

Signature
Controller of Examinations
 Shri Vaishnav Vidyapeeth
 Vishwavidyalaya, Indore

Signature
Registrar
 Shri Vaishnav Vidyapeeth
 Vishwavidyalaya, Indore

Signature
Vice Chancellor
 Shri Vaishnav Vidyapeeth
 Vishwavidyalaya, Indore